Examination SS2017
Communication Systems and Protocols

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Communication Systems and Protocols

Date: 31.07.2017
Name: Test Name
Matr. ID: 1234567
ID: 1

Lecture Hall: ITIV
Seat: 1

Prerequisites for the examination

Aids:

- A single sheet of A4 paper with **self- and hand-written** notes. Writing may be on both sides
- A dictionary
- A not-programable calculator.
- Writing utensils
- Use only indelible ink - use of pencils and red ink is prohibited.
- Other material than that mentioned above, is strictly forbidden. This includes any type of communication to other people.

Duration of the examination:

The exam duration is 120 minutes.

Examination documents:

The examination comprises 32 pages (including title page, 8 blocks of tasks).
Answers may be given in English or German. A mix of language within a single (sub)-task is not allowed.
Please check your matriculation number and id on every page before processing the tasks.
In your solution mark clearly which part of the task you are solving. Do not write on the backside of the solution sheets. If additional paper is needed ask the examination supervisor.

End of Exam:

You will not be allowed to hand in your examination and leave the lecture hall in the last 30 minutes of the examination. At the end of the examination: Stay at your seat and put all sheets (including this title page) into the envelope. Only sheets in the envelope will be corrected. We will collect the examination.

Solution

Task 1: Physical Basics

15

Task 1.1: Drivers

2

A) Insert the logic level (HIGH, LOW) of the output and the state of the transistors (conducts, blocks) into the table according to the input configuration x_1 and x_2 at the standard TTL output driver.

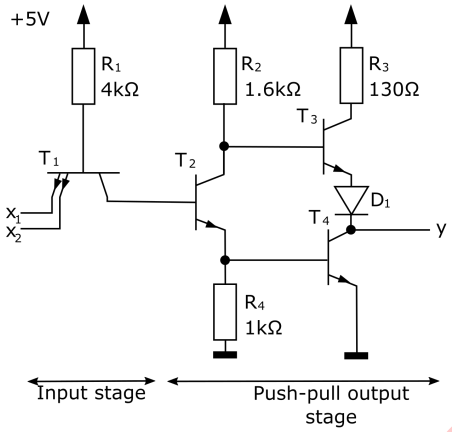


Figure 1.1:

x_1	x_2	T_1	T_2	T_3	T_4	y
0	0	conducts	blocks	conducts	blocks	H
1	1	blocks	conducts	blocks	conducts	L
0	1	conducts	blocks	conducts	blocks	H
1	0	conducts	blocks	conducts	blocks	H

-0.5pt per wrong cell, consider consequential errors

B) List two advantages when using TTL drivers.

1

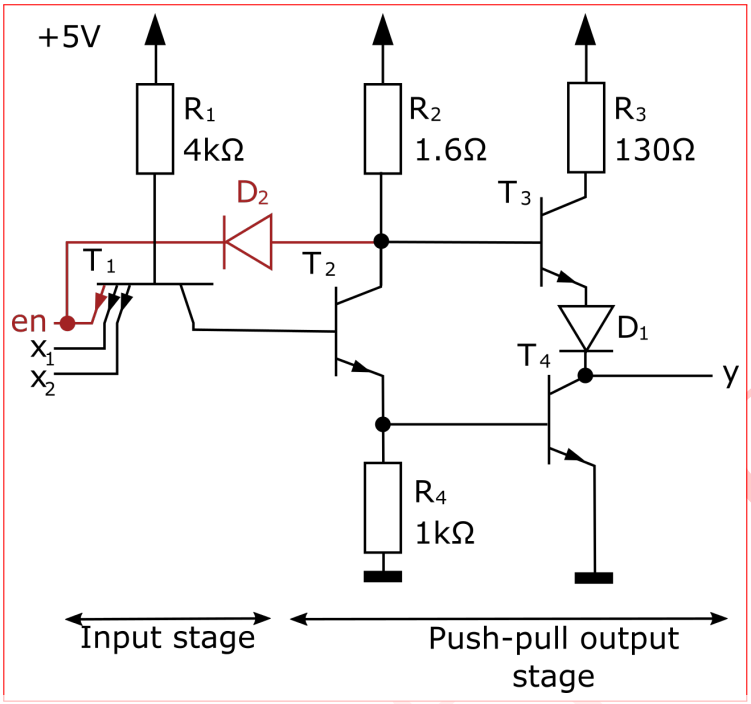
High currents are possible or lower output resistance;
Decouple voltage domains (internal low voltage, external high voltage)
Valid H and L areas are wider

0.5pt per advantage

solution

C) You want to overcome the disadvantage of possible short circuits of a standard TTL driver. Which part of the TTL driver needs to be modified? Modify the drawing to get the solution and describe the purpose of each adjustment made.

2



T1 needs an enable input. Additionally a diode in reverse direction is needed between enable and collector of T2. It should prevent the transistor T_3 from conducting when the enable input is HIGH.

1pt for correct drawing, 0.5pt for description of enable, 0.5pt for description of diode.

Task 1.2: Sampling

When implementing an AD-converter the first step is the sample&hold gate. An example is given in figure 1.2.

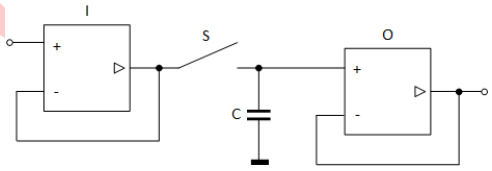


Figure 1.2: Sample&Hold gate

A) Why is such a gate required for the AD conversion process?

1

Solution

The conversion takes time. The signal is not allowed to change during the conversion. Therefore the value of the input signal has the be kept stable by the sample&hold gate.

1pt for keeping signal stable

B) Briefly describe the purpose of every subblock (I, O, S, C) of the sample & hold gate. What is its function inside the sample & hold gate?

4

1pt per correct subblock

C The capacitor stores the voltage level of the signal that is to be converted

S Using the switch, the capacitor is loaded up to the value of the signal to be converted

I The impedance converter at the input makes sure that no current is draw from the input signal that would distort the original value

O The voltage follower avoids a change in the voltage stored on the capacitor if the next stage draws current from the output

Solution

Task 1.3: Reflections on wires

In figure 1.3 a transmission system is given. It consists of a voltage source (including an internal resistance R_i), a signal line of length l and a resistor R_L as receiver. The signal propagates with speed v.

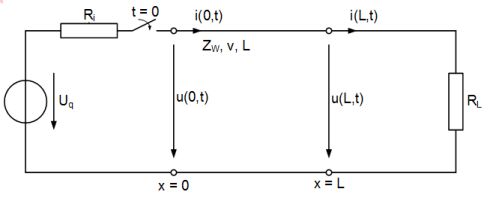


Figure 1.3: Transmission system

For varying R_i and R_L the following signal diagrams (figure 1.4) can be drawn. They are showing the voltage $u(0,t)$ at the beginning of the signal line and the voltage $u(L,t)$, that can be measured at the end of the line.

A) In which of the given examples from figure 1.4, if any, is the line terminated correctly with a suitable value of R_L? Justify your answer.

1

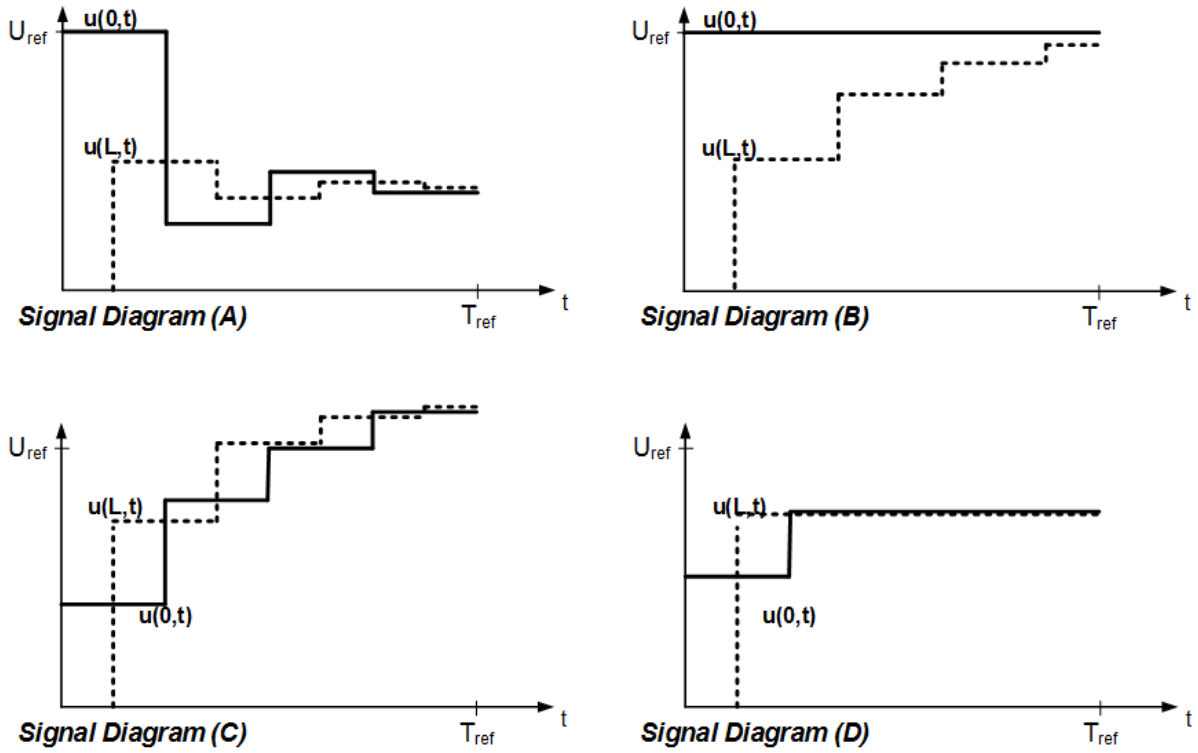


Figure 1.4: Voltages on signal line

In none of the cases, because in each of the examples there are reflections at the end of the line. **1pt for correct answer**

Solution

4

B) For each of the signal diagrams denote the following:

- Is the reflection factor r_i at the beginning of the signal line negative, positive or zero?
- Is the reflection factor r_L at the end of the signal line negative, positive or zero?

Complete the following table accordingly.

0.5pt per correct cell

	r_i **[neg, pos, 0]**	r_L **[neg, pos, 0]**
Signal diagram (A)	pos ($r_i = +0.5$)	neg ($r_L = -0.5$)
Signal diagram (B)	neg ($r_i = -1$)	neg ($r_L = -0.5$)
Signal diagram (C)	pos ($r_i = +0.5$)	pos ($r_L = +0.8$)
Signal diagram (D)	0 ($r_i = 0$)	pos ($r_L = +0.5$)

Solution

Task 2: Transmission Principles

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Task 2.1: Line Codes

A) Why are line codes preferred over baseband signal transmission? In addition, please name and explain two advantages of line codes.

1

Baseband signals can only be used to encode the value of a bit. However line codes support more features like
error detection: signal errors are detectable on the signal level itself.
Multi-valued signals: in a single value more than one symbol can be encoded.
Clock-Recovery: necessary in clock free communication systems

0.5p for each advantage

B) Draw the digital signals for the bit string 011 000 110 100 using each digital encoding scheme. Use Figure 2.1.

2

0.5p for each correct line code; mirrored signal with AMI and NRZI-M is also correct.

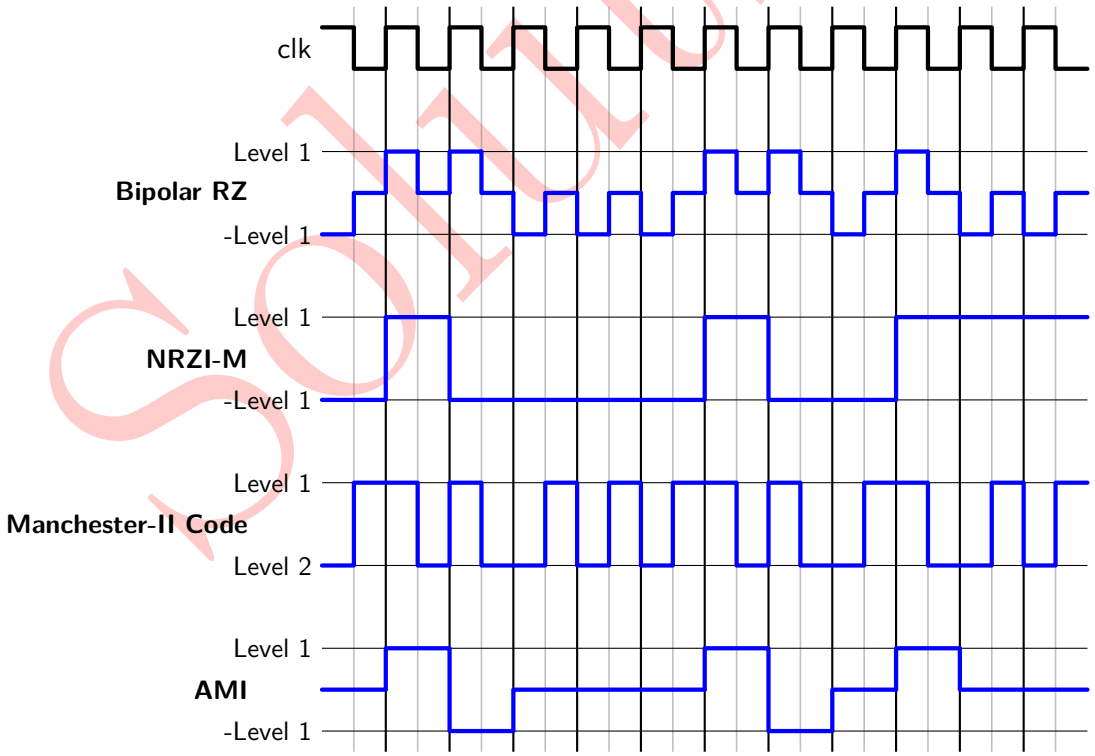


Figure 2.1: Line codes

Solution

C) Classify the line codes given in Table 2.1 according to the properties given in Table 2.1. Use the options given in square brackets only! If requested, please justify your answer below!

6

+0.5pt. per correct answer. Where requested, only with justification!

Line Code	Avg. baud rate compared to bit rate [>=/<=/equal]	Clock Recovery [yes/no]	Error Detection Capability [yes/no]
NRZ	equal	no	no
Bipolar RZ	>=	yes	yes
Manchester-II	>=	yes	yes
AMI	<=	no	yes

Table 2.1: Line code properties

Clock Recovery:
NRZ: no, since signal transitions only occur at interval boundary
Bipolar RZ: yes, since signal transitions to ground level occur in every second half of the bit interval
Manchester-II: yes, since at least one signal transition occurs per bit interval
AMI: yes, if there are no long '0'-sequences via missing polarity change

Error Detection Capability:
NRZ: no, since there is only a direct assignment of a bit to a signal level over the entire bit interval
Bipolar RZ: yes, missing return to zero in the middle of the bit interval
Manchester-II: yes, missing signal transition in the middle of the bit interval
AMI: yes, no change in polarity in successive mark ('1')

Solution

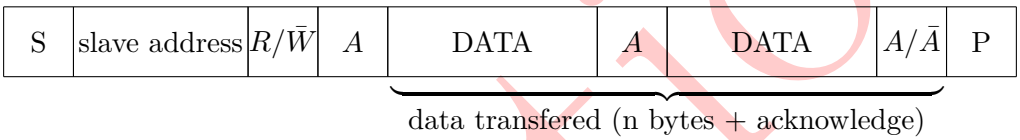
D) What problems can occur, if a transmission line is not DC balanced? Name two problems. **1**

1.) When transmitting data and power supply voltage over the same line, the supply voltage is affected. 2.) When using transducers as couplers, varying DC affects data interpretation on receiver's end.

0.5p for each correct explanation.

Task 2.2: I²C Arbitration

In this task we want to investigate the data transmission on the I²C-Bus. The simplified packet format is given in Figure 2.2. Three master nodes are simultaneously trying to transmit or read one byte of data to or from different slaves over the I²C-Bus.



term	descripion
S	start condition
slave address	7-bit slave address
$R/\bar{W}$	read/write: read 1, write 0
A	acknowledge from slave ('0')
$\bar{A}$	not acknowledge ('1')
DATA	8-bit data
P	stop Condition

Figure 2.2: I²C-Bus frame format

A) What condition must be met during regular data transmission concerning the SCL and SDA line? Which erroneous behavior would occur, if this condition is violated? Justify your answer! **1**

The SDA signal value should not change while SCL is high, otherwise a false stop condition is detected.

+0.5p for condition. 0.5p for consequence of false stop.

Solution

B) The addresses of the slaves, communication mode (R/$\overline{W}$) and the data to be send or read to or from them is shown in the Table 2.2. Complete the signal diagram in the Figure 2.3.

4

node	slave address	R/$\overline{W}$	data
Master 1	1001001	0	$0x15$
Master 2	0101100	1	$0x81$
Master 3	0101101	0	$0x45$

Table 2.2: I^{2}C Communication Parameters

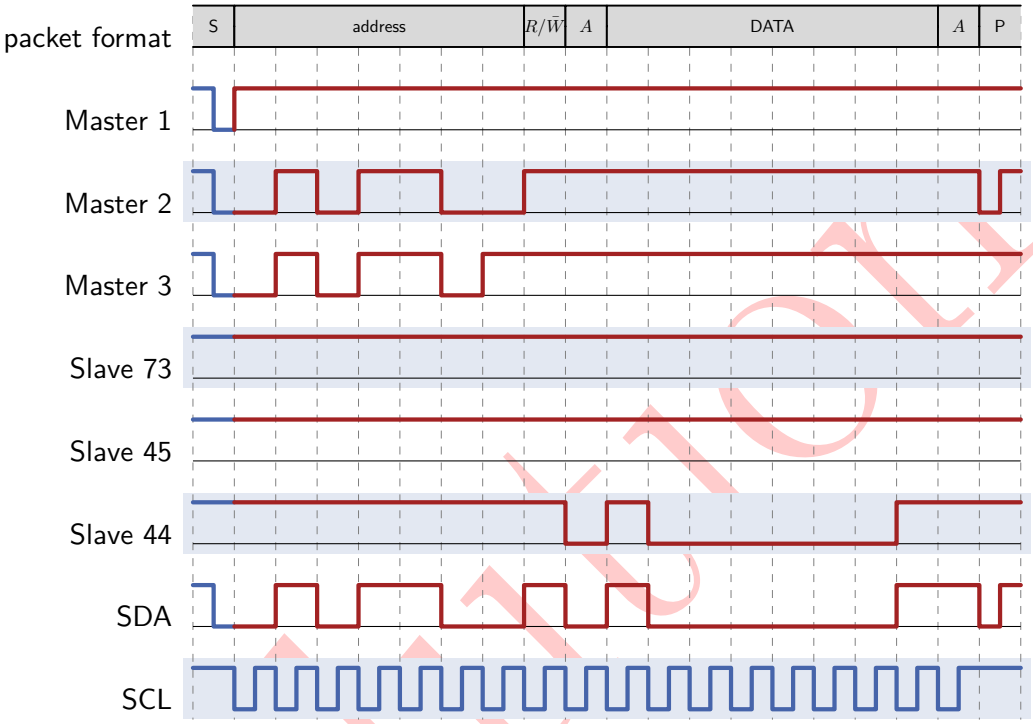


Figure 2.3: Signal sequence

C) How many nodes can be connected to the I^{2}C bus at maximum? Justify your answer!

1

Maximum of $2^7 = 128$ nodes can be connected to the bus when neglecting the reserved addresses in the 7 bit address tag of the I2C frame.

+1P only with justification! 128-16 reserved addresses = 112 is also correct!

Solution

13

Task 3: Modulation and Spread Spectrum

Task 3.1: Modulation

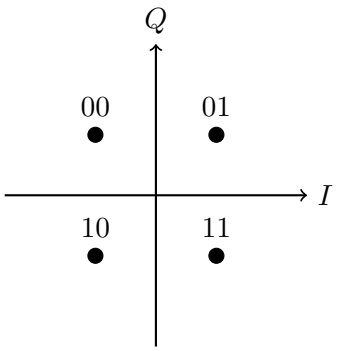


Figure 3.1: The constellation diagram of a certain modulation

A) The constellation diagram of a certain modulation is shown in the Figure 3.1.Which modulation schemes may be used? 1

Phase-Shift Keying (PSK),Quadrature Amplitude Modulation (QAM)

0.5 point for PSK, 0.5 point for QAM

B) By assuming that you have a bistream of information, i.e. **101011000111...**, which you want to modulate using 64-Quadrature Amplitude Modulation (64-QAM) Technique. How many bits for each symbol do you need to use to construct a 64-Quadrature Amplitude Modulator? 1

6 (six) bits

one point or nothing

Solution

4

C) A constellation diagram of 4-QAM is shown below (Figure 3.2). You have information bits **00111010** which will be processed from the left to the right. The Figure 3.3 shows the in-phase carrier signal (B), in-phase symbol (A), and in-phase modulated signal (C). Moreover, the Figure 3.4 shows the quadrature carrier signal (E), quadrature symbol (D), quadrature modulated signal (F). Sketch waveforms to the Figure 3.3 (A and C) and Figure 3.4 (D and F) which resemble symbol representations and modulated information signals seen from in-phase and quadrature axes. The symbol period is twice as long as the period of carrier signal.

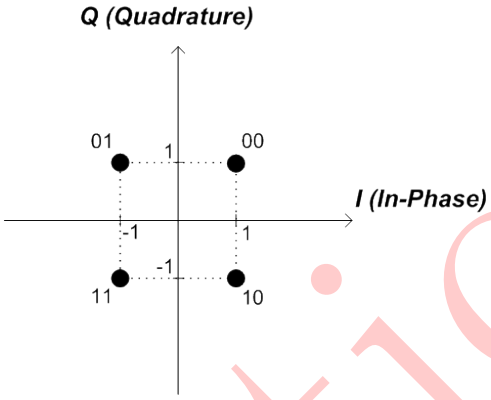
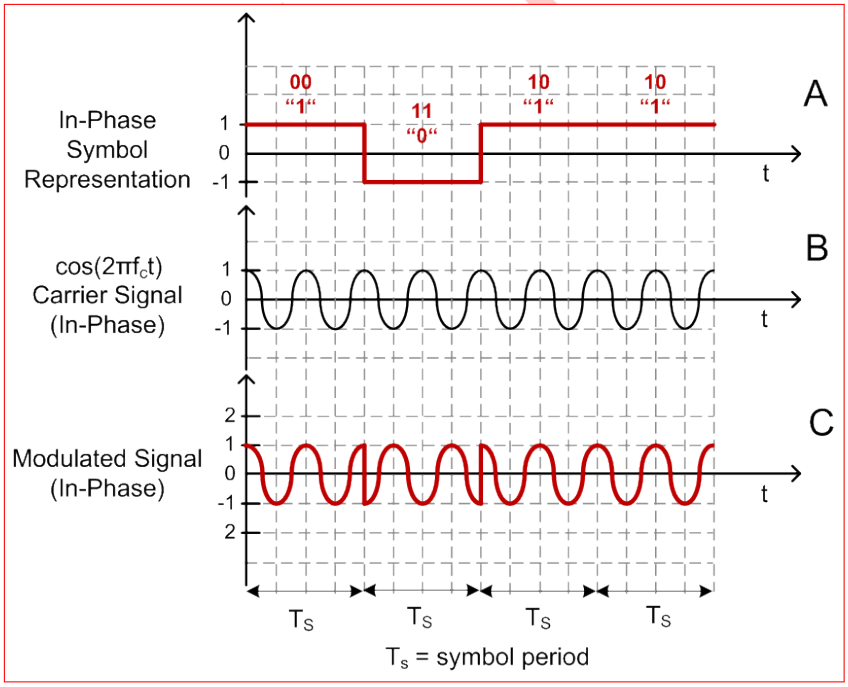
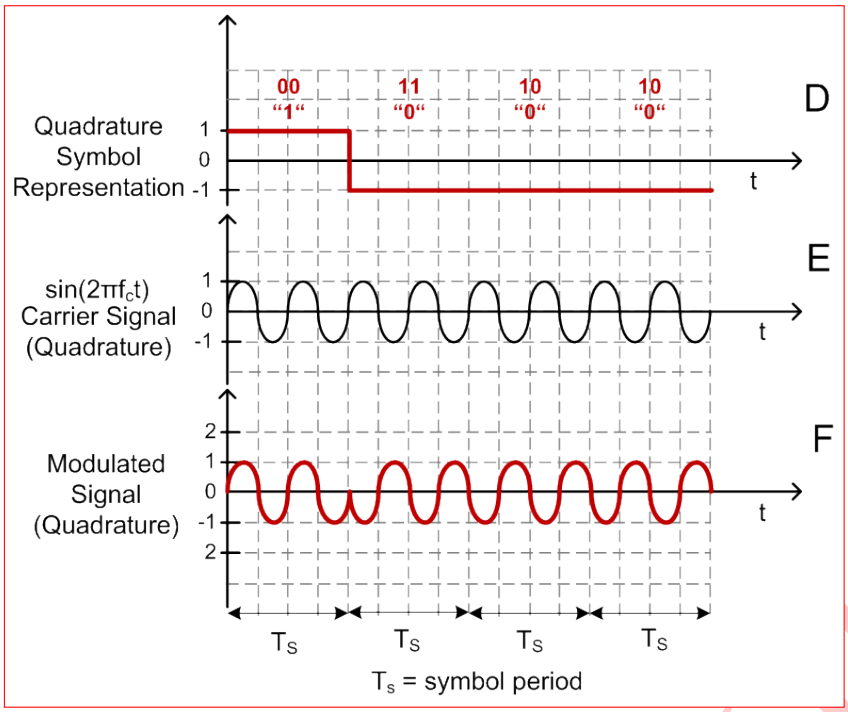


Figure 3.2: A constellation diagram of 4-QAM



1 point for the Sketch A
1 point for the Sketch C

Figure 3.3: In-Phase symbol representation, carrier signal (in-phase), and modulated signal (in-phase)



1 point for the Sketch D
1 point for the Sketch F

Figure 3.4: Quadrature symbol representation, carrier signal (quadrature), and modulated signal (quadrature)

Task 3.2: Spread Spectrum

A) In communication systems, spread spectrum technique is commonly used due to some advantages. To show the influence of spread sprectrum technique to the bandwidth of a signal, the amplitude of a signal and the bandwitdth of the signal can be also sketched in frequency domain. If the power density of a signal is proportional to the square of the amplitude of the signal, which signal does represent after spread and before spread referring to Figure 3.5?

1

Signal bandwidth A: before spread
Signal bandwidth B: after spread

0.5 point: if part of the answer states "Signal bandwidth A is before spread"
0.5 point: if another part of the answer states "Signal bandwidth B is after spread"

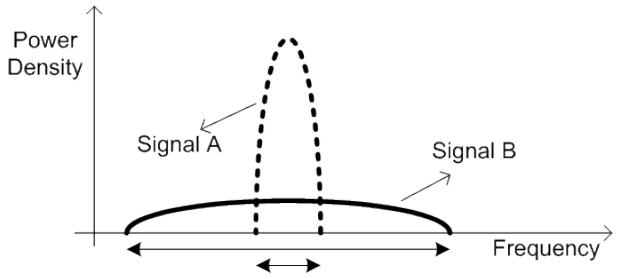


Figure 3.5: A representation of signal's power densities vs. signal's frequencies

Solution

B) What are the requirements for spreading codes used by CDMA?

1

The spectrum of the spread data function shall look like white noise

Spreading functions have to be orthogonal (orthogonal means that the inner product of two functions equals to 0)

0.5p for each requirement

node	function							
0	+1	+1	+1	+1	+1	+1	+1	+1
1	+1	-1	+1	-1	+1	-1	+1	-1
2	+1	+1	-1	-1	+1	+1	-1	-1
3	+1	-1	-1	+1	+1	-1	-1	+1
4	+1	+1	+1	+1	-1	-1	-1	-1
5	+1	-1	+1	-1	-1	+1	-1	+1
6	+1	+1	-1	-1	-1	-1	+1	+1
7	+1	-1	-1	+1	-1	+1	+1	-1

Table 3.1: Walsh sender functions

C) For the simultaneous transmission of four messages, the Walsh function presented in Table 3.1 shall be used. The nodes 0, 2, 5 and 7 transmit data according to Table 3.2. Give the resulting signal on the media, make use of the given scheme in 3.2.

3

0.5p per correct line +0.5p if everything is correct

Node	Data	Signal							
0	"0"	+1	+1	+1	+1	+1	+1	+1	+1
2	"1"	-1	-1	+1	+1	-1	-1	+1	+1
5	"1"	-1	+1	-1	+1	+1	-1	+1	-1
7	"0"	+1	-1	-1	+1	-1	+1	+1	-1
Signal on media		0	0	0	+4	0	0	+4	0

Table 3.2: transmission with CDMA

Solution

D) The following Signal has been received from a transmission using the Walsh functions from this task. **2**

+0.9 +1.2 -3.4 -2.5 +0.9 +1.2 +1.1 +0.8

As corruptions might happen during transmission, the receiver has a tolerance band for the detection. All values differing up to ±0.5 from the ideal value will still be accepted. Calculate the bit value that the receiver will detect for node 3 and node 6.

0.5p for each correct sum
0.5p node 3: no detection
0.5p node 6: for detect zero

Node 3

Received	+0.9	+1.2	-3.4	-2.5	+0.9	+1.2	+1.1	+0.8
Node 3	+1	-1	-1	+1	+1	-1	-1	+1
	+0.9	-1.2	+3.4	-2.5	+0.9	-1.2	-1.1	+0.8

sum 0 → no information was transmitted by node 3.

Node 6

Received	+0.9	+1.2	-3.4	-2.5	+0.9	+1.2	+1.1	+0.8
Node 6	+1	+1	-1	-1	-1	-1	+1	+1
	+0.9	+1.2	+3.4	+2.5	-0.9	-1.2	+1.1	+0.8

sum +7.8 is in the tolerance band → a zero has been detected.

Solution

16

Task 4: Media Access

Task 4.1: Ethernet

Ethernet is a family of computer networking technologies commonly used in local area networks (LANs) and metropolitan area networks (MANs). Systems communicating over Ethernet divide a stream of data into shorter pieces called frames. Each frame contains source and destination addresses, and error-checking data so that damaged frames can be detected and discarded. The "Carrier Sense Multiple Access with Collision Detection" scheme is used to control access to the shared medium.

A bus system with several nodes is using the Ethernet standard with a transmission rate of $10 Mbit/s$ and a signal speed of $2.5 \cdot 10^8 m/s$. A maximum distance of $2.5 km$ for two nodes has to be considered.

A) Why is it necessary to establish a minimal packet length?

1

A minimal packet length is necessary to detect a collision.

1pt for collision detection

B) Calculate the resulting minimal package length in bits for the bus system.

2

minimal time on the line for one package: $t = \frac{2 \cdot l}{v} = \frac{2 \cdot 2.5 km}{2.5 \cdot 10^8 \frac{m}{s}} = 2 \cdot 10^{-5} s$

minimal package length: $PL \geq t \cdot TR = 2 \cdot 10^{-5} s \cdot 10 Mbit/s = 200 bit$

1pt for 2 times the length
1pt for correct amount of bits

Solution

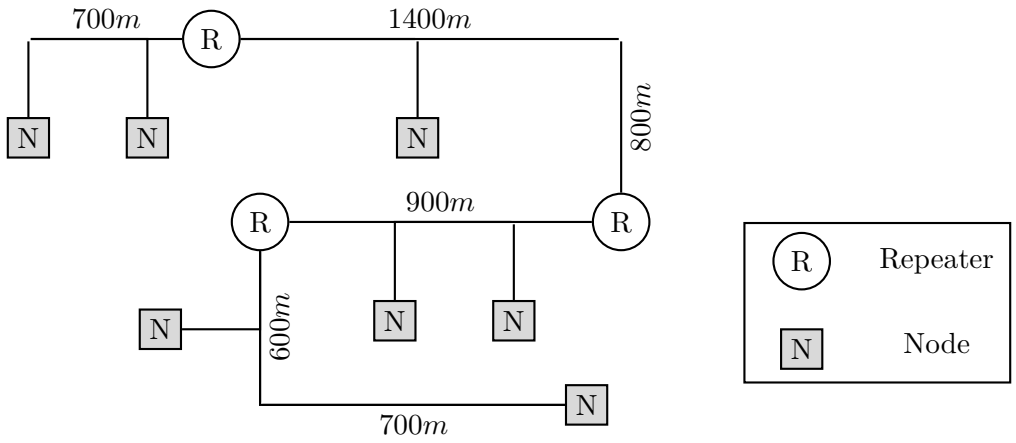


Figure 4.1: Ethernet topology

C) A minimal package length of 64 bytes for the bus system is determined. The bus system is illustrated in figure 4.1 and is used with a transmission rate of $10 Mbit/s$ and a signal speed of $2 \cdot 10^8 m/s$. Each repeater will add a delay of three bits. Is this bus system working with these constraints? Give an explanation! **3**

$PL \geq t \cdot TR = \frac{2l}{v} \cdot TR \Leftrightarrow l \leq \frac{PL \cdot v}{2 \cdot TR}$

$\Rightarrow l \leq \frac{PL \cdot 2 \cdot 10^8 m/s}{2 \cdot 10 Mbit/s} = 10 \frac{1}{bit} \cdot PL$

A delay of 3*3*2 bits has to be considered.

FIRST SOLUTION:
$\Rightarrow l + l_{delay} \leq 10 \frac{m}{bit} \cdot PL$
with $l_{delay} = \frac{18 bits \cdot v}{TR} = 360m$ and $l = 5100m$

$\Rightarrow 5100m + 360m \leq \frac{PL \cdot v}{2 \cdot TR} = \frac{PL \cdot 2 \cdot 10^8 m/s}{2 \cdot 10 \cdot 10^6 bit/s} = 10 \frac{m}{bit} \cdot PL$ with $PL = 512bit$
$\Rightarrow 5460m \leq 5120m$
$\Rightarrow$ A secure detection of collisions is not possible

SECOND SOLUTION
$PL = 512bits - (3 \cdot 3 \cdot 2bits) = 494bit$
$\Rightarrow 5100m \leq 4940m$
$\Rightarrow$ A secure detection of collisions is not possible

THIRD SOLUTION
minimal paket length: $t_s = 2 \cdot \frac{l}{v} = 51 \mu s$
$\Rightarrow PL_{min} = 51 \mu s \cdot TR + delay = 510bits + delay$
A delay of 3*3*2 bits has to be considered
$\Rightarrow PL_{min} = 51 \mu s \cdot TR + 18bits = 528bits$
$\Rightarrow PL_{min} \leq PL$
$\Rightarrow 528bits \leq 512bits$
$\Rightarrow$ A secure detection of collisions is not possible

1pt for correct ansatz
1pt for correct delay
1pt for correct solution

Solution

Task 4.2: CSMA/CA

A communication system comprises five communication nodes that use CSMA/CA as arbitration scheme. In order to transmit data a node transmits a dominant start bit (‚0‘) for synchronization purpose. After that a 5 bit message identifier followed and 10 bits of payload data is sent. The message identifiers are unique for each node and all data is sent MSB first. The bus has to cover a maximum distance of $500m$.

A) Which requirements have to be fulfilled in order to guaranty a faultless function of the system? What are the implications for the transmission rate? **1**

The requirement of simultaneity has to be fulfilled.
The signal propagation time t_s is much smaller compared to the digit length (bit time) t_b:
$\left[t_s = \frac{l}{v}\right] << \left[t_b = \frac{1}{TR}\right]$.

+0.5P for Simultaneity
+0.5P for Transmission rate formula or explanation

B) Table 4.1 shows the identifier of each node. Perform the arbitration phase and fill out the timing diagram in Figure 4.2. **3**

Node	identifier
A	01010
B	00101
C	11001
D	10010
E	00110

Table 4.1: Specification of nodes

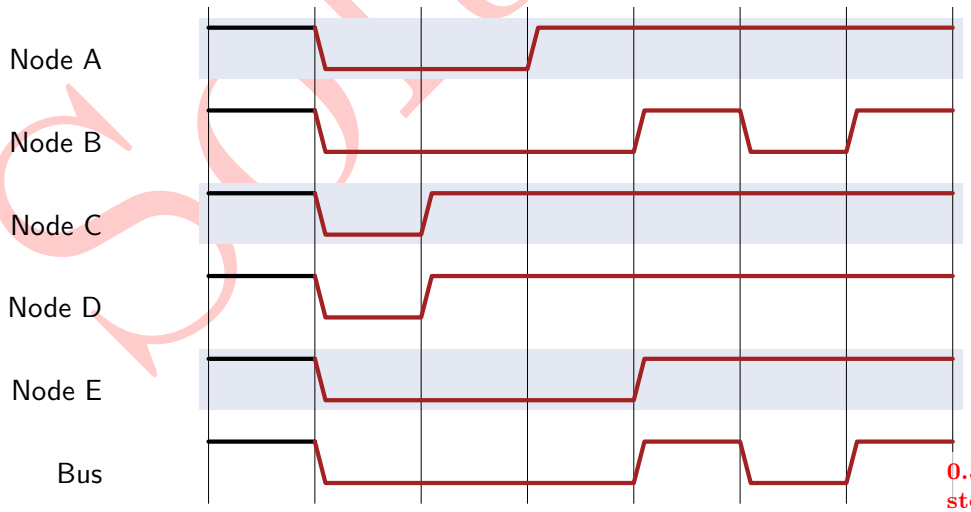


Figure 4.2: Bus Access

0.5P for correct time step (including SOF), no subsequent failure, except SOF missing or dotted line is a failure

C) Which node is granted exclusive access to the bus? **1**

Solution

Node B

1P only for correct answer

Task 4.3: Arbitration

A system using polling is shown in Figure 4.3. An exemplary arbitration cycle of the system is shown in Figure 4.4.

A) Assign the correct signals of Figure 4.3 to the signals shown in the diagram below (Figure 4.4). Justify your choice of signal assignment with a few sentences. What node is sending data at which point in time? Complete the diagram (Figure 4.4) accordingly.

5

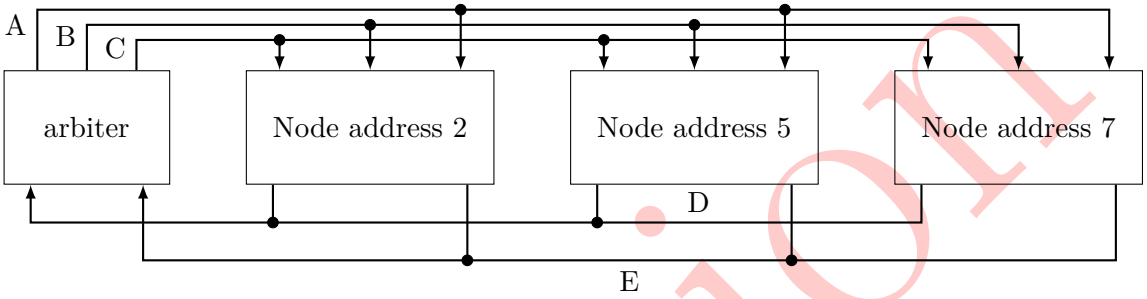


Figure 4.3: Polling

signals D/E - busy and request
A,B,C - address lines

1 Point: assign D/E
1 Point: assign A/B/C
no points if there is no explanation
1P for each correct sender

Solution

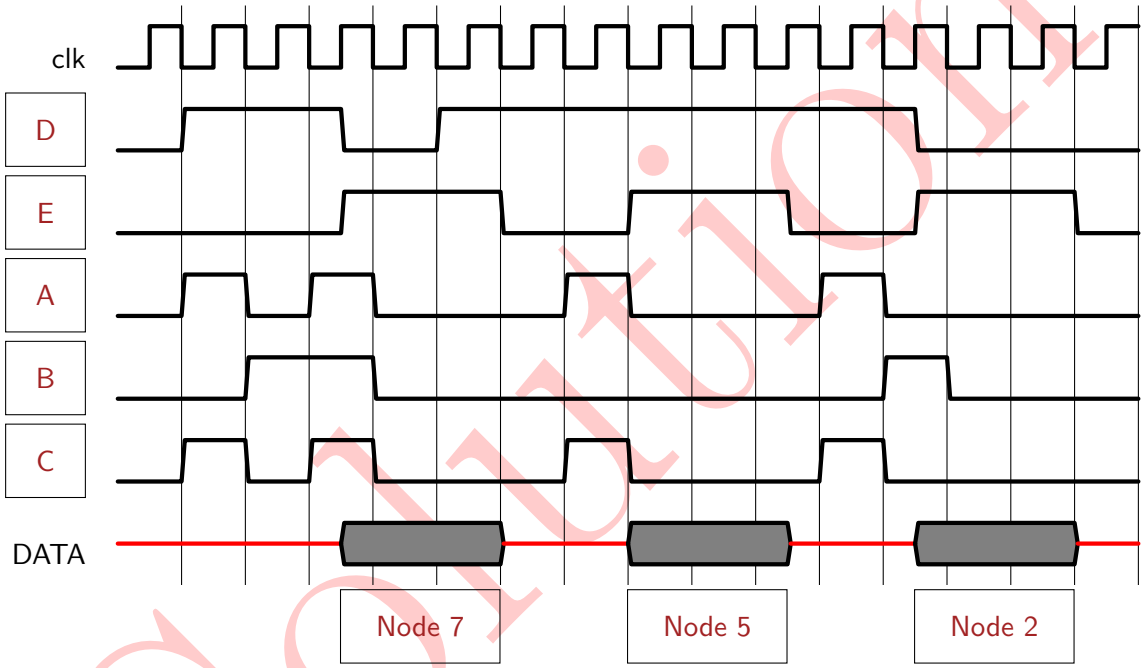


Figure 4.4: Signal flow for Polling

Solution

15

Task 5: Error Protection

Task 5.1: Multiple Choice

3

A) Specify whether the statements in table 5.1 are true or false.
Hint: Wrong answers will be penalised. The task will be evaluated with a minimum of 0 points.

+0,5P each correct answer
-0,5P each wrong answer

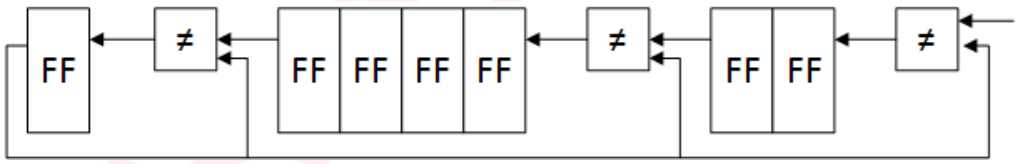
Statements	True	
The receiver has to use a different CRC generator polynomial than the sender		
In a good hash function for communication purposes, a small change in input value results in a small change in hash value		
The Arbitration Field of a CAN massage defines the priority of the message	Yes	
If a CRC generator polynomial G(x) contains factor (x+1), all odd number of bit errors are detectable by the CRC method	Yes	
All error bursts > degree of the CRC generator polynomial are detectable		
Safety is the protection against malicious errors caused by attackers		

Table 5.1: Multiple Choice

Task 5.2: CRC-Calculation

1

A) To protect data transmission in a mobile device, the given CRC generator polynomial should be implemented. Draw the simplified form of the linear feedback registers with XOR operators for the given generator polynomial.
Given CRC generator polynomial: $x^7 + x^6 + x^2 + 1$



+1P everything is correct

Solution

B) Calculate the data stream that will be transmitted if the following bit stream is to be protected using the CRC generator polynomial: $x^7 + x^6 + x^2 + 1$.
Data stream for transmission: **1010 1110**

3

1010	1110	0000	000	:	1110	0101
1100	0101					
0110	1011	0				
110	0010	1				
000	1001	1000				
	1100	0101				
	0101	1101	0			
	110	0010	1			
	0011	1111	10			
	11	0001	01			
		1110	110			

Bit stream as it is transmitted: 1010 1110 1110 110

2pt: calculation correct
0pt if systematic error
1pt if single calculation error
0pt if more than 1 calculation error
1pt for correct complete transmitted bitstream

C) In a transmission system that uses CRC for error detection, a receiver receives the following bitstream: **1010 1001 0001**
Carry out the CRC error detection scheme of the receiver, assuming that the generator polynomial $x^4 + x^2 + 1$ has been used to generate the checksum at the sender. What does the receiver conclude from the result?

2

1010	1001	0001	:	10101
1010	1			
0000	0001	0001		
	1	0101		
	0	0100		

The receiver assumes that an error occured during transmission.

1,5pt: calculation correct
0pt if systematic error
1pt if single calculation error
0pt if more than 1 calculation error
0,5pt for the correct statement

D) Specify the correct bit stream, assuming that only one bit error has occurred in the transmitted bitstream of the task 5.2 C).

1

correct bitstream: 1010 1001 0101

1pt if correct

Solution

Task 5.3: CAN Bus

A) In CAN bus communication it is very important that every participant is able to count the errors. Please give a short explanation why any erroneous participant must be recognized and deactivated. **1**

Malfunctioning participants can bring the complete bus to a deadlock by persistent transmission of error flags

1 pt.: for correct description of complete deadlock

B) In a fresh restarted CAN bus communication system only one node acts as sender and transmits a CAN message every 10 ms. Assume that in every 2nd transmission the sender does not receive an ACK (without a following error flag). Assume further that the first successful transmission is done at t = 0 ms. How long does it take until the sender node switches into the Error Passive state? (Hint: After error: $TX_{CNT} = TX_{CNT} + 8$, after successful transmission $TX_{CNT} = TX_{CNT} - 1$, Condition for transition from Error Active to Error Passive state: $TX_{CNT} > 127$) **3**

After every error -> TX CNT = TX CNT + 8
after every successful transmission TX CNT = TX CNT - 1
Condition for transition from Error Active to Error Passive state:
TX CNT > 127
–> 128 / (8-1) = 18,28... -> after 18 * 2 + 1 = 37 transmissions
–> 37 * 10 ms = 370 ms

+2pt for calculation (# msg)
+1pt for correct answer in ms

C) How long does it take until the sender node switches into the Bus Off state (same conditions as in task 5.3 B)? Please justify your answer. **1**

never! –> If an error passive sender recognizes an ACK error (without a following error flag) the send counter is not incremented any more

+1pt for correct answer

Solution

15

Task 6: Protocols

Task 6.1: FireWire Arbitration

The FireWire network shown below is given.

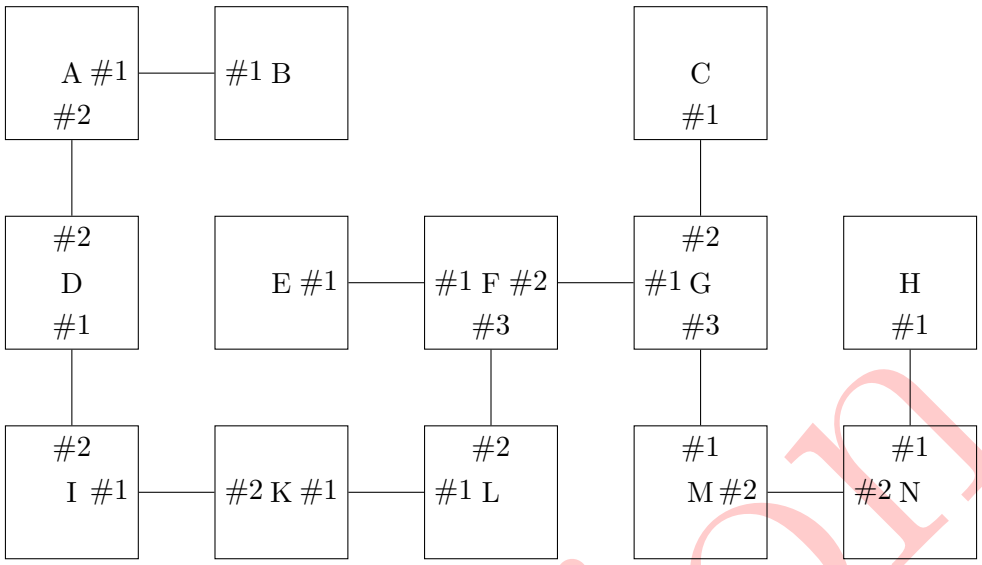


Figure 6.1: FireWire network

A) Mark the root of the FireWire Network in Figure 6.1. 2

L is root. 1pt for correct root

Now a normal FireWire bus cycle should be considered. For simplification, several assumptions should be taken into account:

- A list of nodes wanting to send is given.
- All nodes start requesting the bus at the same time.
- Processing of arbitration request is done in zero time. There are no additional delays for propagation of the arbitration decision.
- If a node receives multiple bus request, it will always forward the request that it receives from the port with the lowest number.

B) The following nodes request access to the bus: **B, C, E, F, H, N**. Determine the order in which the nodes will be granted access to the bus. 2

B, F, E, C, N, H 2pt for correct order

Solution

C) FireWire uses a special coding scheme with an additional STROBE signal. Explain the purpose of the this signal and a possible implementation. **1**

Either Data or Strobe changes its logical value in one clock cycle, but never both. This allows for easy clock recovery with a good jitter tolerance. Implementation by XORing the two signal line values.

0.5pt for purpose
0.5pt for implementation

Task 6.2: Serial Peripheral Interface Bus (SPI)

The Serial Peripheral Interface bus (SPI) is a synchronous serial communication bus specification used for short distance communication.

The SPI bus specifies the following logic signals:

- **SCLK**: Serial Clock (output from master).
- **MOSI**: Master Output Slave Input (data output from master).
- **MISO**: Master Input Slave Output (data output from slave).
- **SS**: Slave Select (active low, output from master).

To begin communication, the bus master configures the clock, using a frequency supported by the slave device. The master then selects each slave device with a logic level 0 on the individual select line. If a waiting period is required, the master must wait for at least that period of time before issuing clock cycles. During each SPI clock cycle, a full duplex data transmission occurs between master and each slave device. The master sends a bit on the MOSI line (using NRZ code) and the slave reads it, while the slave sends a bit on the MISO line and the master reads it. This sequence is maintained even when only one-directional data transfer is intended. In this case the other data sequence is arbitrary. Slave devices have tri-state outputs so their MISO signal becomes high impedance when the device is not selected, because SPI all drivers have push–pull outputs.

A) Name one advantage and one disadvantage of using Slave Select signals for accessing a device. **2**

Advantage: no protocol overhead for transmitting an address

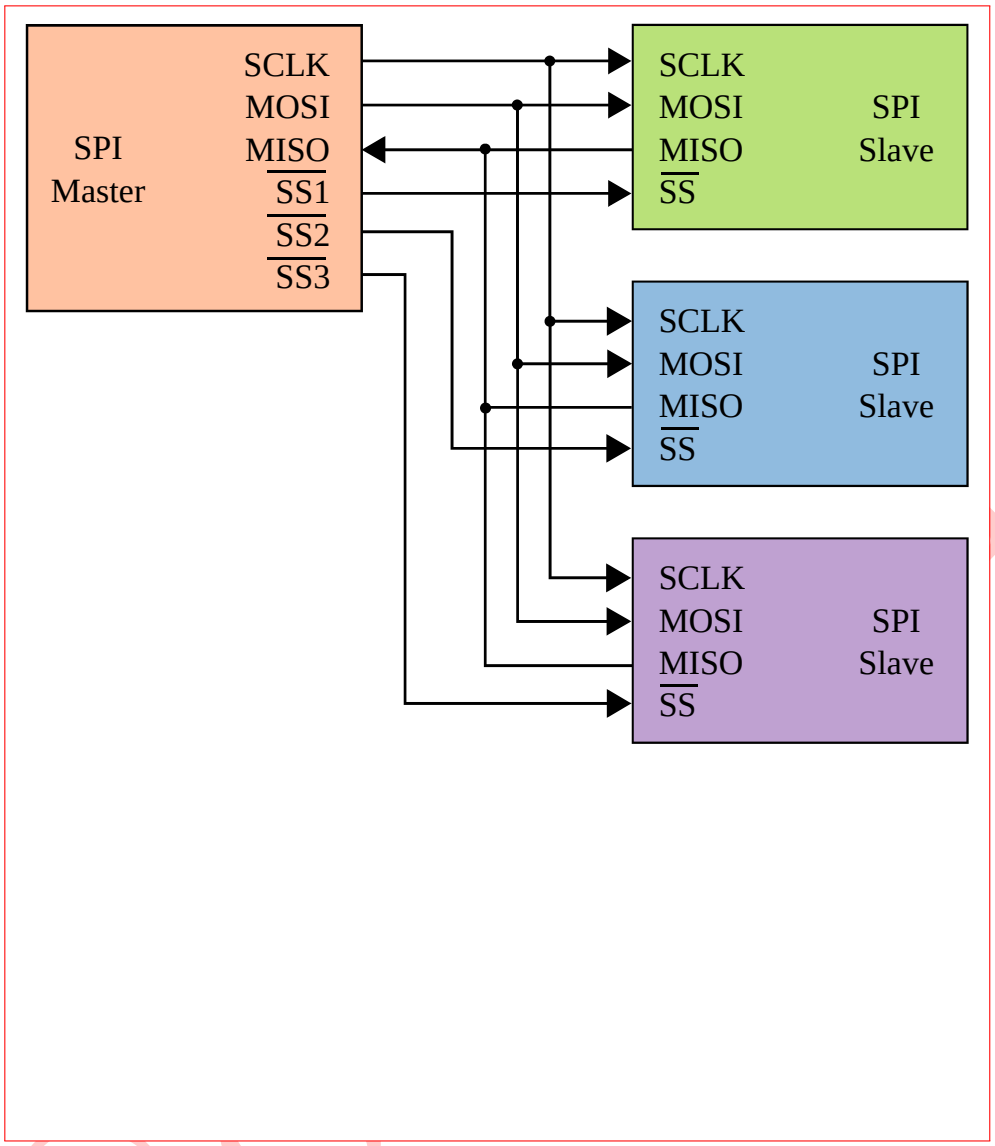
Disadvantage: additional pins need for master and slave devices.

1pt for advantage
1pt for disadvantage

Solution

B) The following diagram shows a single master to a **single** slave configuration. Draw an appropriate diagram for a single master to a **three** slaves configuration below.

3



1pt for bus connection of SCLK, MOSI, MISO
1pt direct slave access (no daisy-chaining)
1pt for additional SS interfaces

C) Draw the timing diagram for the case that the following data byte (given in binary notation) should be transmitted to a single slave: 01011100_b. Thereby the slave sends back the data byte: 10011001_b.
Assume the data captured and output on the clock's rising edge. Use figure 6.2.

3

1pt for corrent SS signal
1pt for correct MOSI signal
1pt for correct MISO signal

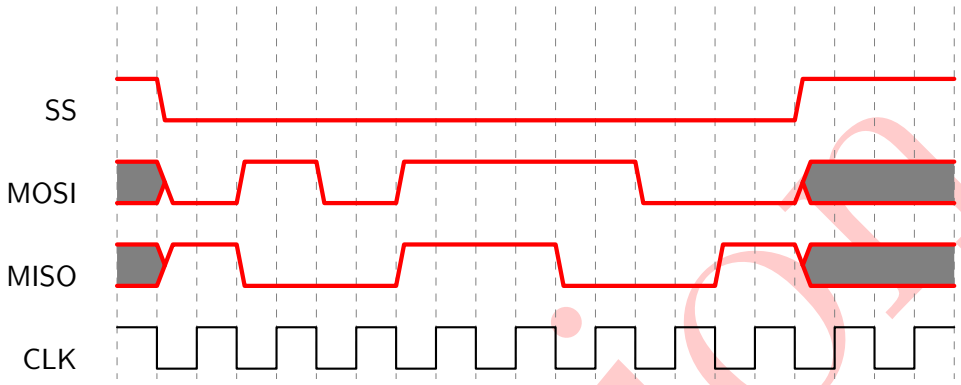


Figure 6.2: SPI full-duplex operation timing diagram

D) Figure 6.3 shows a SPI read operation from a single slave. Add an appropriate SS signal to the diagram and write down the data the master **reads** from the slave in binary notation. Assume the data captured and output on the clock's rising edge.

2

01010100_b

1pt for corrent data
1pt for correct SS signal

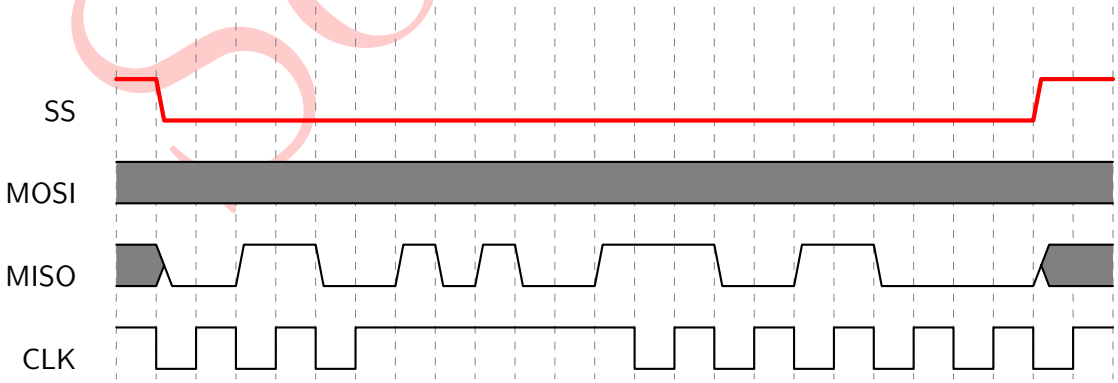


Figure 6.3: SPI read operation timing diagram

Solution

14

Task 7: Routing

Task 7.1: General Questions

A) Explain the three terms hop and diameter in the context of routing.

2

Hop : Data transmission between neighboring nodes. Or Distance. **each one Point**
Diameter : Maximum number of hops between any pair of nodes in a network. Minimal Path of the maximum distance.

B) Explain what the manhattan distance is and in which network topologies it makes sense.

1

Manhattan Distance : physical distance that follows towards the target in a mesh based network **one Point**

C) Explain the term channel in the context of routing. Is it possible to have several channels between the same pair of nodes and explain how this could work ?

2

Channel : logical connection between nodes **all or nothing**
Yes with different physical paths through the network are used.

Solution

D) Describe a network scenario in which routing during design time is favorable compared to routing during runtime and justify your answer ! **2**

Several Answers : **all or nothing**

Communication between nodes has to be as fast as possible, fast pathfinding helps

defective nodes are not possible, fixed paths dont have to be adjusted

complete traffic during runtime is known beforehand, fixed routing suffices network traffic so no adaptive change is needed

E) Describe what kind of information is needed by each router when adaptive routing is used and justify your answer ! **2**

knowledge about the network's status is necessary, otherwise no routing decision during runtime can be made. **all or nothing**

Info about connection to neighbours and metric

Solution

Task 7.2: Dijkstra's Algorithm

A) Explain the term minimal routing and describe a scenario in which non-minimal routing is preferred ! **1**

minimal : shortest path
non-miminal preferred : miminal path has high congestion
several answers failing links

all or nothing, only 1
example -> nothing

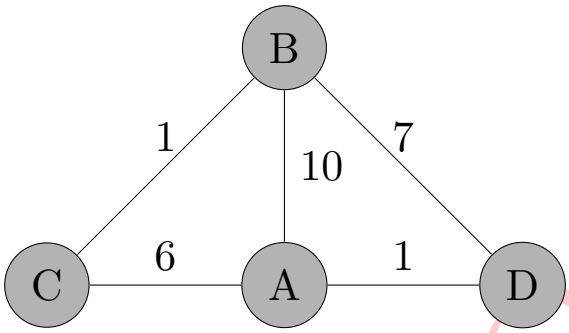


Figure 7.1: Given network topology

B) With node A as the starting point, calculate the shortest paths in the network shown in Figure 7.1, by using Dijkstra's algorithm. For that write down the order in which nodes are visited in each bracket under the current step and fill out the given tables that encompass the shortest paths after each visitation of a node. **4**

	step 1		step 2		step 3		step 4		step 5	
node	**A**		A		D		C		B	
vertex	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.
A	∞	A	0	A	0	A	0	A	0	A
B	∞	-	10	A	8	D	7	C	7	C
C	∞	-	6	A	6	A	6	A	6	A
D	∞	-	1	A	1	A	1	A	1	A

Table 7.1: Dijkstra's algorithm

Each Column 1Pt

Solution

Task 8: Network Topologies

16

Task 8.1: General Questions

A) Is the dijkstra algorithm more suitable for a regular topology (e.g. torus) or an irregular topology (e.g. the topology of the internet)? Choose one and justify your decision!

1

Dijkstra is applicable for both topologies but it is more complex to implement and requires more resources than other solutions available in a regular topology. This makes it better suited for an irregular topology.

Alternative solutions are possible. The reasoning needs to be sound. No points without reasoning! . 0,5 Points for just "it is suitable for both"

B) There are four topologies given: Mesh, Torus, Star, Ring. Assume for each topology a network with 16 nodes. Order the topologies in the given table from best (top) to worst (bottom) regarding the given metric. Metrics: edge connectivity, diameter, resource cost(i.e. in this case the total amount of links in the network). Hint: Think about what is desirable for each metric in a network when deciding the order.

3

Edge Connectivity	Diameter	Resource Cost
Torus	Star	Star
Mesh	Torus	Ring
Ring	Mesh	Mesh
Star	Ring	Torus

Table 8.1: Metrics and topologies

for each collumn: +1 in case all correct, +0.5 in case of one missing topology, 0 Points for more than one missing or one error in the ordering

Solution

Task 8.2: 4D Topology

Meshed topologies offer a very suitable solution for future many-core architectures, especially because of the easy routing scheme available (x,y-based routing). When we increase the amount of nodes in a mesh, it can be useful to scale the mesh into a higher dimension instead of adding the nodes in the same dimension. A higher dimension keeps the diameter low while increasing the edge connectivity of the nodes.

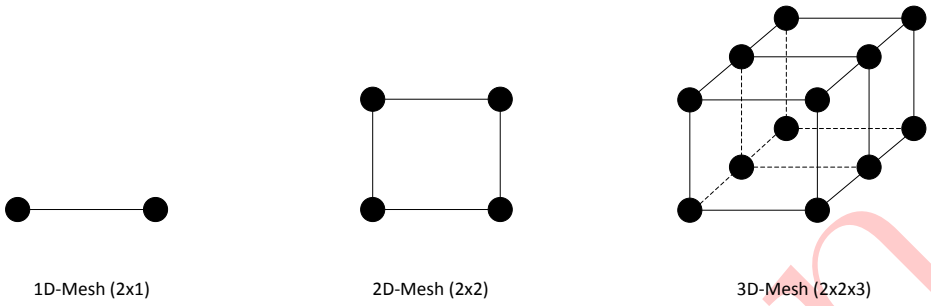


Figure 8.1: Drawing higher-dimensional meshed networks

Mathematically speaking, higher dimensional meshed topologies behave the same as lower dimensional topologies. For drawing them on a sheet of paper, some techniques exist. If we consider a 1-dimensional topology consisting of two nodes and want to move towards a 2-dimensional (2x2) topology, we simply copy our original nodes and connect each node with their exact copy. For a 2x2x3 topology, we copy the existing 2x2-rectangle two times (resulting in 3 rectangles) and connect each original node with their first copy and their first copy with the second copy. The same technique can be applied to a 4D topology, where we copy our 3D cubes and connect each node to its next copy.

Solution

A) Assume a 2x3x4x5 mesh topology for this task. Each node can be described by the tuple (x1,x2,x3,x4). Find the shortest path from the source point (1,1,3,0) to the destination point (0,2,0,3). Thereby, the routing policy that each node has to obey is described as follows: **4**

1. Try first to route in the direction of the largest vector component ($\|\Delta x1\|$, $\|\Delta x2\|$, $\|\Delta x3\|$ or $\|\Delta x4\|$) from the local position towards the destination.
2. In case there are multiple directions with the same largest value for the respective vector components possible, choose the direction of the previous step.
3. In case none of the above rules is possible, prioritize first x1 then x2 then x3 and finally x4 among the directions with the largest vector components.

In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence.

(1,1,2,0) -> (1,1,2,1) -> (1,1,2,2) -> (1,1,1,2) -> (1,1,0,2) -> (0,1,0,2) -> (0,2,0,2) -> (0,2,0,3)

+0.5 pts per intermediate step (start and end point are optional and don't give extra points)
+1 pt for a full solution with no errors

B) Can the routing policy described in the previous question A result in a livelock? Justify your answer! **1**

Lifelock is not possible since all the steps of the algorithm only move towards the target and never away.

+1 pt for Livelock. Explanation may be short but must be present.

C) Explain the difference between a livelock and a deadlock in a network. **1**

In a livelock, the system still continues but a transmission never reaches its destination (due to e.g. circles) while in a deadlock, the system is stuck due to mutual blocking of links.

+1 pt for Explanation

Solution

D) What is the edge connectivity and the diameter of a 2x3x4x5 meshed topology? Shortly justify your answer. **2**

edge connectivity = 4 ,any node at a corner has one connection in each dimension.

diameter = 10 , the shortest path between the two nodes that are the furthest from each other (i.e. diameter) must switch the maximum possible amount of states in each dimension. In this case it is 1+2+3+4 = 10

+1 for each answer, only with reasonable explanation

E) Assume now that there may be broken nodes which may not be selected by a routing algorithm. To cope with these broken nodes, there is an additional rule that extends the first rule and which says: **4**

1. In case a selected direction is not routable (due to the target node being broken), choose among the remaining directions the one of the next largest vector component from the local position towards the destination.

Furthermore assume that there are two broken nodes: (1,1,2,0) and (0,1,1,3). Route a packet again starting from (1,1,3,0) towards (0,2,0,3) and name all visited nodes on the way.

(1,1,3,1) -> (1,1,2,1) -> (1,1,1,1) -> (1,1,1,2) -> (1,1,1,3) -> (1,2,1,3) -> (0,2,1,3) -> (0,2,0,3)

+0.5 pts per intermediate step (start and end point are optional and don't give extra points)
+1 pt for a full solution with no errors

Solution